REMARKS

Claims 4, 5, 7, 10, 14, 17 and 18 are pending in the present application. Claims 1-3, 6, 8, 9, 11-13, 15, 16 and 19-21 were previously canceled.

Applicant respectfully requests reconsideration of the application in view of the remarks appearing below, which Applicant believes shows that the application is in condition for allowance.

Response to Arguments

In the current Office Action, in responding to Applicant's argument that electrostatic charge is not considered a surface contaminant the U.S. Patent and Trademark Office (USPTO) argues that Applicant is incorrect in distinguishing surface contaminants from static electrical charge. In the context of the present invention and present claims, Applicant respectfully disagrees.

Asserting That Static Electrical Charge Is A Surface Contaminant Violates Canons Of Construction That Differing Claim Elements Are Presumed To Have Differing Meanings And That Words and Phrases In The Same Claim Should Not Render Other Words And Phrases In That Claim Superfluous

One basic canon of claim construction is that differing words and phrases used in the same claim have differing meanings. *See, e.g.*, Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc., 381 F.3d 1111, 1119-20 (Fed. Cir. 2004) ("when an applicant uses different terms in a claim it is permissible to infer that he intended his choice of different terms to reflect a differentiation in the meanings of those terms.") Another basic canon of claim construction is that words and phrases in a particular claim should not be construed in a way that renders other words or phrases superfluous. *See, e.g.*, Primos, Inc. v. Hunter's Specialties, Inc., 451 F.3d 841, 848 (Fed. Cir. 2006) ("the terms 'engaging' and 'sealing' are both expressly recited in the claim and therefore 'engaging' cannot mean the same thing as 'sealing'; if it did, one of the terms would be superfluous.")

In the present case, independent claim 17 states "a conductive rotating wafer-cleaning member operatively configured to engage said surface of microelectronics wafer in said wafer cleaning region so as to remove contaminants from said surface and provide part of a grounding path between said microelectronics wafer and said electrical ground for removing electrical charge from said microelectronics wafer." Emphasis added. The conductive rotating wafer-

cleaning member of claim 17 has two functions, namely, removing contaminants from the surface of the wafer and removing static electrical charge from the wafer. Clearly, the USPTO's argument that static electrical charge is a contaminant renders the "contaminants" limitation superfluous. Thus, the USPTO argument that a static electrical charge is a contaminant simply cannot stand.

Similarly, independent claim 10 is directed to a "method of removing surface contaminants from a surface of a microelectronics wafer that may have a static electrical charge thereon" comprising cleaning said surface of said microelectronics wafer with a conductive rotating wafer-cleaning member so as to remove at least some of the surface contaminants, and so as to simultaneously create an electrical ground path between said surface and an electrical ground through said conductive rotating wafer-cleaning member." Emphasis added. Here, too, it is clear that the "static electrical charge" limitation cannot simply mean "surface contaminants." Otherwise, the "contaminants" limitation becomes superfluous.

Asserting That Static Electrical Charge Is A Surface Contaminant Vitiates The Dual Functionality Of The Conductive Rotating Wafer

The entire present application and claims are directed to removing both static electrical charge and surface contaminants that are mechanically removed by a cleaning member. If the USPTO's argument were correct and there were no non-static electrical charge contaminants, then the mechanical contaminant-removal aspect of the cleaning member would be rendered superfluous.

Skilled Artisans In The Relevant Field Of Technology Recognize A Distinction Between Static Electrical Charge And Surface Contaminant

A simple online search, such as a Google search, conducted, for example, using the search phrase "electrostatic charge contaminant" reveals that those skilled in the semiconductor field do not view a "static charge," i.e., an excess or dearth of electrons, as a "surface contaminant." Electrons are sub-atomic particles, whereas surface contaminants are super-atomic particles. While electrostatic charge on a wafer can increase the amount of contaminants on the wafer because of electrostatic attraction, the charge itself is not considered a contaminant. See, for example, the attached excerpts from chapter 5, "Contamination Control" of Microchip Fabrication, A Practical Guide To Semiconductor Processing," Peter Van Zant, McGraw Hill, 4th Ed., 2000. Applicant respectfully asserts that anyone skilled in the art reading the current application and claims would understand that static electrical charge is not a contaminant.

For at least the foregoing reasons, Applicant respectfully requests withdrawal of the USPTO's assertion that static electrical charge is a type of surface contaminant in the semiconductor-wafer-cleaning context of the present claims.

Rejections Under 35 U.S.C. § 103(a)

Hawn/Lur/Kitamura

Claims 10 and 17 stand rejected under 35 U.S.C § 103(a) as being obvious in view of a combination of the Hawn IBM Technical Disclosure Bulletin (hereinafter "Hawn"), U.S. Patent No. 6,743,721 to Lur et al. (hereinafter "Lur"), and U.S. Patent No. 5,508,879 to Kitamura et al. (hereinafter "Kitamura"). The USPTO asserts that Hawn teaches (1) a system for discharging unwanted potentials on a dielectric surface and (2) grounding a conductive brush which contacts the dielectric surface. The USPTO further asserts that Lur teaches that a wafer comprises dielectric surfaces and silicon surfaces. Hawn further teaches electrically grounding the apparatus with an electrically conductive path extending from the article to the ground. Applicant respectfully disagrees with the present rejection.

The Hawn Bulletin describes removing unwanted electrostatic charges from photoconductive plates using a soft grounded brush with multiple conductive points that come into intimate contact with the surface being discharged.

Lur discloses a microelectronics wafer having a dielectric surface.

Kitamura discloses a charge removal brush that includes a number of long, conductive filamentous elements for removing charges from an object when the charge removal brush comes in contact with the object, is disclosed.

Turning now to the rejected claims, independent claim 10 as previously presented includes the limitation of "cleaning said surface of said microelectronics wafer with a conductive rotating wafer-cleaning member so as to remove at least some of the surface contaminants, and so as to simultaneously create an electrical ground path between said surface and an electrical ground through said conductive rotating wafer-cleaning member." [Emphasis added.] Similarly, independent claim 17 as previously presented includes the limitation of "a conductive rotating wafer-cleaning member operatively configured to engage said surface of microelectronics wafer in said wafer cleaning region so as to remove contaminants from said surface and provide part of a grounding path between said microelectronics wafer and said electrical ground for removing electrical charge from said microelectronics wafer." [Emphasis added.]

Surface contaminants include "particles, mobile ions and trace metals, among others, that are remnants of the various processes used to make the articles or are otherwise present in the manufacturing environment." (¶0002) As discussed above in the previous section, surface contaminants are distinguishable from electrostatic charge. It is well understood that discharge of surface potential involves draining off excess electrons, which are quantum entities that may not be physically translated merely by brushing with macroscopic fibers. Applicant respectfully submits that surface contaminants would be understood by one having ordinary skill in the arts to encompass larger particles subject to more classical physics.

Hawn does not mention surface contaminants. Kitamura teaches removal of excess or extraneous toner particles (Kitamura, Col. 7, L. 22-24), but these are particles intentionally introduced to the surface and are highly uniform in size and surface chemistry, and are not a result of the manufacturing process or manufacturing environment. Thus neither Hawn nor Kitamura teach removal of surface contaminants. Therefore the Hawn/Kitamura combination does not teach all of the essential elements of claim 10 or claim 17.

The USPTO asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the brush of Hawn with the rotating brush of Kitamura so that the brush will be capable of effectively removing charges from the surface of the wafer, and so the brush will provide an efficient cleaning operation (Kitamura, Col. 5, L. 36-42), and that a rotating brush will allow the brush to remove contaminants more efficiently than a stationary brush.

First, Applicant respectfully disagrees with this motivation for combining the references, especially in light of the fact that neither reference involves removal of surface contaminants, but rather surface electrostatic charge, which again is not a surface contaminate capable of being removed mechanically by brushing action. Second, Applicant does not believe that it is at all obvious that a brush configuration that may be effective and efficient, however those terms may be defined in this circumstance, at removal of electrostatic charge will be equally effective or efficient at removal of surface contaminants.

> A statement that modifications of the prior art to meet the claimed invention would have been "well within the ordinary skill of the art at the time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references.

MPEP 2143.01(IV), citing Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

Applicant respectfully requests the USPTO provide references which support the asserted motivation for combining and modifying the teachings of electrostatic grounding of Hawn and Kitamura, such as the assertion of effectiveness and efficiency for a rotating brush, to arrive at the claimed obviousness of the surface contaminant removal of Applicant's claims.

Hawn and Kitamura are directed toward removal of unwanted surface charge, and not to removal of surface contaminants, and the differences between the nature of static charge and surface contaminants make the motivations or suggestions for modifying the combined references nonsensical. For at least the foregoing reasons, Applicant respectfully requests that the Examiner withdraw the present rejection.

Hawn/Kitamura/ConductivePlastics.com

Claims 4 and 5, 7, 14, and 18 stand rejected under 35 U.S.C § 103(a) as being obvious in view of a combination of the Hawn and Kitamura references, each discussed above, and further in view of Conductiveplastics.com. Applicant respectfully disagrees.

The Hawn Bulletin, Lur et al., and Kitamura references are as described above relative to the obviousness-type rejection.

The Conductiveplastics.com Webpage discloses a conductive polyurethane foam touted for its cleanliness, i.e., lack of sloughing and particulation.

As discussed above relative to the obviousness-type rejection in view of the Hawn/Lur/Kitamura combination, Applicant believes that at least the teachings of the combination and the proposed motivation for modifying these teachings to read upon the claim limitations is improper relative to claims 10 and 17. The additional combination with the Conductiveplastics.com Webpage, in Applicant's view, does not remedy the shortcomings of this improper combination. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)." MPEP §2143.03. Consequently, it is Applicant's position that the Hawn/Lur/Kitamura/Conductiveplastics.com combination does not render claims 18, 14, 7, 4 or 5 obvious.

For at least this reason, Applicant respectfully requests that the Examiner withdraw the present rejection.

CONCLUSION

In view of the foregoing, Applicant submits that claims 4, 5, 7, 10, 14, 17 and 18 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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By: _____

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Attachments:

Excerpts from Peter Van Zant, Microchip Fabrication, A Practical Guide To Semiconductor Processing," McGraw Hill, 4th Ed., 2000.

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electrical power lines, and clean-room materials. Critical-process machines are backed up to the wall dividing the clean room and the bay. This arrangement allows technicians to service the equipment from the back without entering the clean room.

Double-door pass-throughs. The bay also serves as a semi-clean area for the storage of materials and supplies. They are put into the clean room through double-door, pass-through units that protect the cleanliness of the clean room. Pass-through units may be simple double-door boxes or may have a supply of positive-pressure filtered air with interlocking devices to prevent both doors from being opened at the same time. Often the pass throughs are fitted with HEPA filters. All materials and equipment brought into the clean room should be cleaned prior to entry.

Static control. Higher-density circuits with submicron feature sizes are vulnerable to smaller particles of contamination attracted by static to the wafer. Static charges build up on the wafers, the storage boxes, work surfaces, and equipment. Each of these items can carry static charges as high as 50,000 V (volts) that attract aerosols out of the air and from personnel garments. The attracted particles end up contaminating the wafers. Statically held particulates are very difficult to remove with standard brush and wet cleaning techniques.

Most static charge is produced by *triboelectric* charging. This occurs when two materials initially in contact are separated. One surface becomes positively charged as it loses electrons. The other becomes negatively charged as it gains electrons. The triboelectic series table in Fig. 5.16 shows the charging potential for materials some materials found in a clean room.[9]

Static also represents a device operational problem. It occurs in devices with thin dielectric layers, as in MOS gate regions. An electric static discharge (ESD) of up to 10 A (amperes) is possible. This level of ESD can physically destroy an MOS device or circuit. ESD is a particular worry in device-packaging areas. This problem requires that sensitive devices, such as large-array memories, be handled and shipped in holders of antistatic materials.

Photomasks and reticles are particularly sensitive to ESD. A discharge can vaporize and destroy the chrome pattern.

Some equipment problems are static related, especially robots, wafer handlers, and measuring equipment. Wafers usually come to the equipment in carriers made of PFA type materials. This carrier material is chosen for its chemical resistance, but it is not conductive. Charge builds up on the wafers, but cannot dissipate to the carriers. When the carrier comes close to a piece of metal on the equipment,

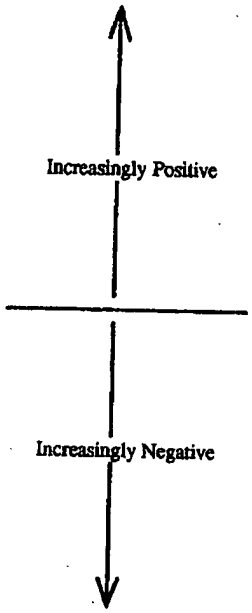

Figure 5.16 Triboelectric series. (*Hybrid Circuit Technology Handbook, Noyes Publications*)

the wafer charge discharges to the equipment. The electromagnetic interference produced interferes with the machine operation.

Static is controlled by prevention of charge build-up and discharge techniques (Fig. 5.17). Prevention techniques include use of antistatic materials in garments and in-process storage boxes. In some areas, a topical antistatic solution may be applied to the walls to prevent the buildup of static charge. These solutions work by leaving a neutralizing residue on the surface. Generally, they are not used in critical stations because of the possible contaminating effect of the residue.

Discharge techniques include the use of ionizers and grounded static-discharge straps. Ionizers are placed just underneath the HEPA filters where they function to neutralize any charge buildup in the filtered air. Ionizers are also placed on nitrogen blow-off guns for the same effect. Some stations will have a portable ionizer blowing ionized air directly on the wafers being processed. Static discharge is also accomplished by grounding operators with wrist straps, having grounded mats at critical stations, and grounding work surfaces. Comprehensive static control programs, with prevention and discharge methods along with personnel training and third party monitoring are a feature in most advanced fabs.

Shoe cleaners. In any contamination controlled area, the dirtiest region is the floor. Removal of dirt from the sides of shoes and shoe coverings is accomplished by shoe cleaners stationed at the clean room

cleaners and applicators, including mops, must be carefully specified. Normal household cleaners are far too dirty for use in clean rooms. Special care must be taken when using vacuum cleaners. Special clean-room vacuums with HEPA filtered exhausts are available. Many clean rooms will have built-in vacuum systems to minimize dirt generation during cleaning.

The wipe-down of process stations is done with special low-particulate wipes and sponges. The wiping procedure is critical. Wall surfaces should be wiped from top to bottom and deck surfaces from back to front. Cleaning chemicals in spray bottles should be sprayed into wipes, not onto the surfaces. This simple procedure minimizes unwanted overspray onto the wafers and equipment. Clean room cleaning has, itself, become a supporting technology to semiconductor processing. Many fabs use outside certification services[24] to identify and document cleanliness levels, practices, documentation and control procedures.

Wafer Surface Cleaning

Clean wafers are essential at all stages of the fabrication process, but are especially necessary before any of the operations performed at high temperature. Up to 20% of all process steps relate to wafer cleaning.[25] The cleaning techniques described here are used throughout the wafer fabrication process.

The story of semiconductor process development is in many respects the story of cleaning technology keeping pace with the increasing need for contamination-free wafers. Wafer surfaces have four general types of contamination. Each represents a different problem on the wafer and each is removed by different processes. The four types are:

1. Particulates
2. Organic residues
3. Inorganic residues
4. Unwanted oxide layers

In general, a wafer cleaning process, or series of processes, must remove all surface contaminants (listed above), does not etch or damge the wafer surface, is safe and economical in a production setting, and is ecologically acceptable. Cleaning processes are generally designed to accomodate two primary wafer conditions. One, called the *Front End of the Line* (*FEOL*), refers to the wafer fabrication steps used to form the active electrical components on the wafer surface. During these steps, the wafer surface, and particularly the gate areas of MOS transistors, are exposed and vulnerable. A critical parameter in these

cleans is *surface roughness*. Excessive surface roughness can alter device performance and compromise the uniformity of layers deposited on top of the devices. Surface roughness is measured in nanometers as the root mean square of the vertical surface variation (nmRMS). Year 2000 requirements are on the order of 0.15 nm, dropping to less than 0.1 nm by the year 2010.[26] Other concerns in FEOL cleaning processes are the electrical condition of the bare surface. Metal contaminants on the surface change the electrical characteriztics of devices, with MOS transistors being particularly vulnerable. Sodium (Na) is a particular problem (see Chapter 4), along with Fe, Ni,Cu, and Zn. Cleaning processes will have to reduce concentrations to less than 2.5×10^9 atoms/cm^2 to meet 2010 device needs. Aluminum and calcium are also problems and need reduction on the surface to the 5×10^9 atoms/cm^2 level.[27]

A most critical factor is maintaining the integrity of gate oxides. Cleaning processes can attack and rough up gate oxides, with the thinner ones most vulnerable. A gate oxide is required to act as a dielectric in a MOS transistor, and as such must have a consistent structure, make up and thickness. Gate Oxide Integrity (GOI) is measured by testing the gate for electrical shorts. The NTRS indicates that at 180 nm, technology levels gates will have to exhibit less than 0.02 defects/cm^2 when tested at 5 MV/cm for 30 seconds.[28]

Specific concerns at the BEOL cleans, in addition to particles, metals, and general contamination are anions, polysilicon gate integrity, contact resistance, via hole cleanliness, organics, and the overall numbers of shorts and opens in the metal system. These issues are explored in Chapter 13. Photo resist removal is also a cleaning process with both FEOL and BEOL consequences. These issues are explored in Chapter 9.

Different chemicals and cleaning methods are mixed and matched to accomodate the needs at particular steps in the process. A typical FEOL cleaning process (such as preoxidation clean) is listed in Fig. 5.23. The FEOL process listed is called a nonHf-last process. Other variations have the HF removal step last. NonHf-last surfaces are hydrophillic that can be dried without water marks and have a thin oxide (grown in the cleaning steps) that can protect the surface. They

- particle removal (mechanical)
- general chemical clean (such as sulfuric acid/H_2/O_2)
- oxide removal (typically dilute HF)*
- organic and metal removal (SC-1)
- alkali metal and metal hydroxide removal (SC-2)
- rinse steps
- wafer drying

Figure 5.23 Typical FEOL cleaning process steps.

also absorb more organic contamination. HF-last surfaces are hydrophobic, which can be difficult to dry without water marks if there are also hydrophillic (oxides) surface layers present. These surfaces are stable from hydrogen surface passivation.[29] A choice of either nonHF-last or HF last depends on the sensitivity of the devices being fabricated in the wafer surface and general cleanliness requirements.

Particulate removal

Particulates on the wafer surface vary from very large ones (50-μm size) to very tiny ones less than a micron in size. The larger ones can be cleaned off by conventional chemical baths and rinses. The smaller particulates are more difficult to remove because they can be held to the surface by several strong forces. One is called the van der Waals force. It is a strong interatomic attraction between the electrons of one atom and the nucleus of another. A technique to minimize electrostatic attraction is manipulation of a factor called the *zeta potential*. Zeta potential arises from a charge zone around particles that is balanced by an oppositely charged zone in the cleaning liquid. This charge varies with velocity (the speed of movement of the cleaning liquid, as when the wafers are moved in a cleaning bath), the pH of the solution, and the concentration of electrolytes in the solution. It is also affected by additives to the cleaning solution, such as surfactants. These conditions can be set to create a large charge that has the same polarity of the wafer, thus creating a repulsion that serves to keep the particle in the solution and off the wafer surface.

Capillary force is another problem. It occurs when there is a liquid bridge between a particle and the surface (Fig. 5.24). Capillary forces can be higher than van der Waals forces.[30] Surfactants and mechanical assist, such as megasonics, are used to dislodge these particles from the surface.

Cleaning processes are most often a series of steps designed to remove both the large and small particles. The simplest particulate removal process is to blow off the wafer surface using a spray of filtered high-pressure nitrogen from a hand-held gun located in the cleaning stations. In fabrication areas where small particles are a problem, the

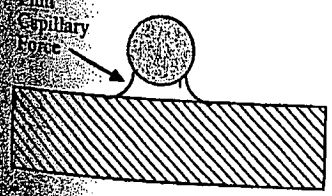

Figure 5.24 Capillary force from film.

nitrogen guns are fitted with ionizers that strip static charges from the nitrogen stream and neutralize the wafer surface.

Nitrogen blow-off guns are effective in removing most large particles. Since the guns are hand-held, the operators must use them in a manner that does not contaminate other wafers in the station or the station itself. Blow-off guns are not generally used in Class 1/10 clean rooms.

Wafer scrubbers

The stringent wafer cleanliness requirements for epitaxial growth led to the development of mechanical wafer surface scrubbers, and are used wherever particulate removal is critical.

The scrubbers hold the wafer on a rotating vacuum chuck (Fig. 5.25). A rotating brush is brought in near contact with the rotating wafer while a stream of deionized water is directed onto the wafer surface. The combination of the brush and wafer rotations creates a high-energy cleaning action at the wafer surface. The liquid is forced into the small space between the wafer surface and the brush ends where it achieves a high velocity, which aids the cleaning action. Caution must be exercised to keep the brushes and cleaning liquid lines clean to prevent secondary contamination. Also, the brush height above the wafer must be maintained to prevent scratching the wafer surface.

Surfactants may be added to the D.I. water to increase the cleaning effectiveness and prevent static build-up. In some applications, diluted ammonium hydroxide may be used as the cleaning liquid to prevent build up of particles on the brush and to control the zeta potential in the system.[31]

Scrubbers are designed as standalone units with automatic loading capabilities or are built into other pieces of equipment to clean the wafers automatically before processing.

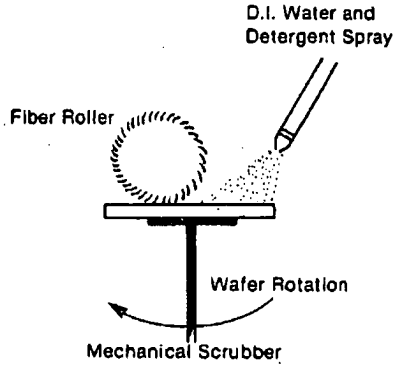

Figure 5.25 Mechanical scrubber.

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Figure 5.25 Mechanical scrubber.

High-pressure water cleaning

The removal of statically attached particles first became a necessity for the cleaning of glass and chrome photomasks. A high-pressure water spray process was developed, using a small stream of water pressurized 2000 to 4000 psi. The stream is swept across the mask or wafer surface, dislodging both large and small particles. Often a small amount of surfactant will be added to the water stream to act as a destatic agent.

Organic residues

Organic residues are compounds that contain carbon, such as oils in fingerprints. These residues can be removed in solvent baths such as acetone, alcohol, or TCE. In general, solvent cleaning of wafers is avoided whenever possible due to the difficulty of drying the solvent completely off the wafer surface. Also, solvents always contain some impurities that may themselves represent a contamination source.

Inorganic residues

Inorganic residues are those that do not contain carbon. Examples are inorganic acids such as hydrochloric or hydrofluoric acid, that may be introduced from other steps in wafer processing. The organic and inorganic residues are cleaned from the wafers in a variety of cleaning solutions described in the following section.

Chemical cleaning solutions

A wide range of cleaning processes exist in the semiconductor industry. Each fabrication area has different cleanliness needs and different experiences with different solutions. The solutions described in this section are those in common use, although there are numerous variations and different combinations of solutions from one fabrication area to another. Described are processes used to clean wafers before doping, deposition, and metallization steps. (The special case of photoresist removal is addressed in Chapter 8.)

Liquid chemical cleaning processes are generally referred to as *wet processes* or *wet cleaning*. Immersion cleaning takes place in glass, quartz, or polypropylene tanks fitted into the deck of a cleaning station (see Chapter 4). Where heating of the solution is required, the tank may be sitting on a hot plate, be wrapped with heating elements, or have an immersion heater inside. Chemicals are also applied by spraying, either using direct impingement or in centrifugal tools (see spin rinse dryers).